WHAT IS CLAIMED IS:

1. A semiconductor contact connection structure comprising:

a insulator substrate;

a first semiconductor device formed on the insulator substrate;

a non-conducting gate interconnect layer formed on the insulator substrate for connecting to a gate of a second semiconductor device; and

a silicide layer formed on the gate interconnect layer, and an active region of the first semiconductor device for making a connection thereof.

2. The connection structure of claim 1 wherein the silicide layer further covers a dielectric edge portion separating the gate interconnect layer from the active region.

3. The connection structure of claim 1 wherein the silicide layer further covers a sidewall of the gate interconnect.

4. The connection structure of claim 1 wherein the first semiconductor device is formed on a silicon based material layer on the insulator substrate wherein the silicon based material layer has a thickness of more than 20 angstroms.

5. The connection structure of claim 1 wherein the active region serves as a local connection layer between the first and second semiconductor devices.

6. The connection structure of claim 1 wherein the silicide layer is less than 350 angstroms in thickness.

7. The connection structure of claim 1 wherein the silicide layer provides an electrical resistance of 100 ohm/ea, or less, between the gate interconnect layer and

the active region.

8. An SRAM cell formed on an insulator substrate, the cell comprising:

at least one active region with a silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of at least a PMOS transistor and an NMOS transistor, the two transistors forming a first inverter; and

a sidewall butted connection structure used in conjunction with a gate interconnect layer for connecting the drain nodes of the transistors of the first inverter to gates of at least two transistors of a second inverter.

9. The cell of claim 8 wherein the active region further connects to a source node of at least one pass gate.

10. The cell of claim 9 wherein the pass gate's drain node is connected to an access line.

11. The cell of claim 8 further comprising a first metal layer for forming wordline metal straps and landing pads for power supply lines and access lines.

12. The cell of claim 11 further comprising a second metal layer for forming power supply lines and access lines.

13. The cell of claim 12 wherein the access lines are interposed between the power supply lines.

14. The cell of claim 11 wherein lines on the first and second metal layers are arranged in a substantially perpendicular fashion.

15. An SRAM cell formed on an insulator substrate, the cell comprising:

a first inverter having a first PMOS transistor and a first NMOS transistor;

a second inverter having a second PMOS transistor and a second NMOS transistor; and

a sidewall butted connection structure used in conjunction with a gate interconnect layer for connecting drain nodes of the transistors of the first inverter to gates of the two transistors of the second inverter.

16. The cell of claim 15 further comprising a first metal layer for forming landing pads for at least one wordline and at least one power supply line or access line.

17. The cell of claim 15 wherein the first metal layer is also used for forming a connection between the drain nodes of the two transistors of the first or second inverter.

18. The cell of claim 16 further comprising a second metal layer for forming at least one wordline metal strap and landing pads for at least one power supply line or access line.

19. The cell of claim 18 further comprising a third metal layer for forming power supply lines and access lines.

20. The cell of claim 19 wherein the access lines are interposed between the power supply lines.

21. The cell of claim 15 further comprising at least one active region with a silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of the transistors of the first inverter.

22. The cell of claim 15 wherein the sidewall butted connection structure is

electrically connected to a source node of a pass gate.

23. The cell of claim 15 further comprising a first metal layer for forming at least one power supply line and at least one access line.

24. The cell of claim 23 further wherein the first metal layer is used for forming landing pads for at least one wordline, or landing pads for at least one power supply line.

25. The cell of claim 23 further comprising a second metal layer for forming at least one wordline metal strap and at least one power supply line.

26. A method for forming a sidewall butted connection structure, the method comprising:

forming an insulator substrate;

forming a first semiconductor device on the insulator substrate, the device having a gate material for forming a gate region over a gate dielectric material and an interconnection layer for connecting to a second semiconductor device;

removing a spacer from a sidewall of the interconnection layer over the active region; and

forming a continuous silicide layer over the active region and the interconnect layer without interruption caused by the sidewall,

wherein the continuous silicide layer connects the active region of the first semiconductor device to the second semiconductor device.

27. The method of claim 26 wherein the removing of a spacer further includes using a lithograph process and an etching process.

28. The method of claim 26 wherein the step of forming the silicide layer further includes:

forming a metal material layer on top of the interconnect layer and the active region; and

annealing the metal material layer to generate the silicide layer.

29. The method of claim 28 wherein the silicide layer includes TiSi2, CoSi2, NiSi, PtSi, or WSi2.

30. The method of claim 28 wherein the gate oxide has a thickness less than 22 angstroms.

31. The method of claim 28 wherein the silicide layer has a thickness less than 350 angstroms.